Listing of Claims

This listing of claims replaces all prior claims of the captioned patent application.

Claim 1. (currently amended) A method for routing ~~at least one~~ a plurality of critical conductors ~~conductor~~ in an integrated circuit design, the method comprising the operations ~~steps~~ of:

identifying ~~providing~~ a plurality of logic signals which are to be communicated by the ~~said at least one~~ critical conductors ~~conductor~~;

prioritizing the plurality of critical conductors by ranking the ~~determining that at least one conductor is a~~ critical conductors in order of the importance of the critical conductors relative to each other, ~~conductor to~~ the importance being with respect to the needs of the critical conductors to be protected ~~protect~~ from inductive coupling or capacitive coupling from at least one adjacent conductor;

providing a plurality of preferred tracks, each track being configured to be located adjacent to ~~determining the location of~~ at least one ~~preferred track, said preferred track adjacent to a~~ constant voltage conductor;

prioritizing the plurality of preferred tracks by ranking the preferred tracks in order of which preferred track is immediately adjacent to the most constant voltage conductors; and

routing the ~~said at least one~~ critical conductors into the preferred tracks according to the rankings of both the critical conductors and the preferred tracks starting with the critical conductor having the highest critical conductor rank being first routed into the ~~said at least one~~ preferred track having the highest preferred track rank ~~; and~~

~~protecting said plurality of logic signals communicated by said at least one~~

~~conductor from inductive coupling or capacitive coupling by routing said at least~~

~~one critical conductor~~ .

Claims 2-3. (canceled)

Claim 4. (currently amended) A computer system for routing conductors in an

integrated circuit design, the computer system comprising:

a processor; and

a memory operatively coupled to said processor, the memory having stored

therein instructions for performing the following operations:

identifying a plurality of the conductors to be connected in an integrated

circuit configured with the design by being placed into tracks having various locations

relative to constant voltage conductors wherein preferred tracks are located

immediately adjacent to one or more of the constant voltage conductors, the

conductors comprising critical conductors that are sensitive to inductive coupling or

capacitive coupling from at least one adjacent conductor;

ranking each of the preferred tracks with respect to all of the other preferred

tracks in an order based on which preferred track is immediately adjacent to the most

constant voltage conductors;

~~means for providing a plurality of logic signals which are~~

~~communicated by said at least one conductor;~~

~~means for determining the number of critical conductors to protect~~

~~from inductive coupling or capacitive coupling from at least one adjacent~~

~~conductor;~~

ranking each of the critical conductors with respect to all of the other critical

conductors in an order based on the importance of protecting each particular critical

conductor from inductive coupling or capacitive coupling from at least one adjacent

conductor; and

~~means for determining the location of at least one preferred track, said~~

~~preferred track adjacent to a constant voltage conductor;~~

~~————— means for~~

routing the ~~said at least one~~ critical ~~conductor~~ conductors into ~~said at least one~~

the preferred tracks ~~preferred track~~ according to the rankings of both the critical

conductors and the preferred tracks, the routing starting with the critical conductor

having the highest critical conductor rank being first routed into the preferred track

having the highest preferred track rank ~~and~~

~~means for protecting said plurality of logic signal communicated by said at~~

~~least one conductor from inductive coupling or capacitive coupling by routing said at~~

~~least one critical conductor~~ .

Claim 5. (currently amended) A ~~The~~ computer system as recited in ~~according to~~

claim 4, wherein the routing operation first routes the critical conductor having the

highest critical conductor rank into the preferred track that is located immediately

adjacent to more constant voltage conductors than are immediately adjacent to

any of the other preferred tracks

~~memory further having stored therein the following~~:

~~means for ranking each of said at least one critical conductor in order of~~

~~importance relative to other critical conductors; and~~

~~means for routing said ranked critical conductors, according to said ranking~~.

Claim 6. (currently amended) A ~~The~~ computer system <u>as recited in</u> ~~according to~~ claim 4, the memory further having stored therein <u>instructions for performing</u> the following <u>operation</u>:

<u>continuing the routing of the</u> critical <u>conductors</u> into <u>the preferred tracks according to the rankings of both critical conductors remaining in the critical conductor ranking and preferred tracks remaining in the preferred track ranking, the routing starting with the next critical</u> conductor <u>having the next highest critical conductor rank being next routed into the preferred track having the next highest preferred track rank</u> ~~and~~

~~means for ranking said at least one preferred track location according to whether said at least one preferred track locations are adjacent to one or more constant voltage conductors; and~~

~~means for routing said ranked critical conductors, according to said track location ranking, and said critical conductor ranking~~ .

Claim 7. (currently amended) A <u>computer program product embodied on a computer-</u>~~machine-~~readable medium <u>and comprising code that, when executed by the computer, causes the</u> ~~disposed on a~~ computer to perform <u>the following for routing conductors</u> ~~a method for routing at least one critical conductor~~ in an integrated circuit design, ~~the method comprising the steps of~~:

<u>identifying a plurality of the conductors to be connected in an integrated circuit configured with the design by being placed into tracks, the tracks having various locations relative to constant voltage conductors, preferred ones of the tracks being located immediately adjacent to one or more of the constant voltage conductors, the conductors comprising critical conductors that are sensitive to inductive coupling</u>

or capacitive coupling from at least one adjacent conductor;

ranking each of the preferred tracks with respect to all of the other preferred tracks in an order based on which preferred track is immediately adjacent to the most constant voltage conductors;

~~providing a plurality of logic signals which are communicated by said at least one conductor;~~

~~determining the number of critical conductors to protect from inductive coupling or capacitive coupling from at least one adjacent conductor;~~

ranking each of the critical conductors with respect to all of the other critical conductors in an order based on the importance of protecting each particular critical conductor from inductive coupling or capacitive coupling from at least one adjacent conductor; and

~~determining the location of at least one preferred track, said preferred track adjacent to a constant voltage conductor;~~

routing the ~~said at least one~~ critical ~~conductor~~ conductors into ~~said at least one~~ the preferred tracks ~~preferred track~~ according to the rankings of both the critical conductors and the preferred tracks, the routing starting with the critical conductor having the highest critical conductor rank being first routed into the preferred track having the highest preferred track rank ~~and~~

~~protecting said plurality of logic signals communicated by said at least one conductor from inductive coupling or capacitive coupling by routing said at least one critical conductor~~ .

8. (currently amended) <u>A computer program product embodied on a computer-readable medium as recited in claim 7, wherein the code, when executed by the computer, causes the computer to further perform the following:</u> ~~The machine-readable medium of claim 7, the method therein further comprising the step of:~~

<u>continuing the routing of the critical conductors into the preferred tracks according to the rankings of both critical conductors remaining in the critical conductor ranking and preferred tracks remaining in the preferred track ranking, the routing starting with the next critical conductor having the next highest critical conductor rank being next routed into the preferred track having the next highest preferred track rank</u>

~~ranking each of said at least one critical conductor in order of importance relative to other critical conductors; and~~

~~wherein said routing step further includes the step of routing said ranked critical conductors, according to said ranking~~ .

Claim 9. (currently amended) <u>A computer program product embodied on a computer-readable medium as recited in claim 8, wherein the code, when executed by the computer, causes the computer to further perform the following:</u> ~~The machine-readable medium of claim 8, the method therein further comprising the step of:~~

<u>continuing the continuing routing until either all of the critical conductors have been routed into one of the preferred tracks according to the rankings of both critical conductors remaining in the critical conductor ranking and preferred tracks remaining in the preferred track ranking, or there are no more preferred tracks in the ranking of preferred tracks</u>

~~ranking said at least one preferred track location according to whether said at least one preferred track location are adjacent to at least one constant voltage conductor; and~~

~~wherein said routing step further includes the step of routing said ranked critical conductors, according to said track location ranking and said critical conductor ranking~~ .